

FIG. 1

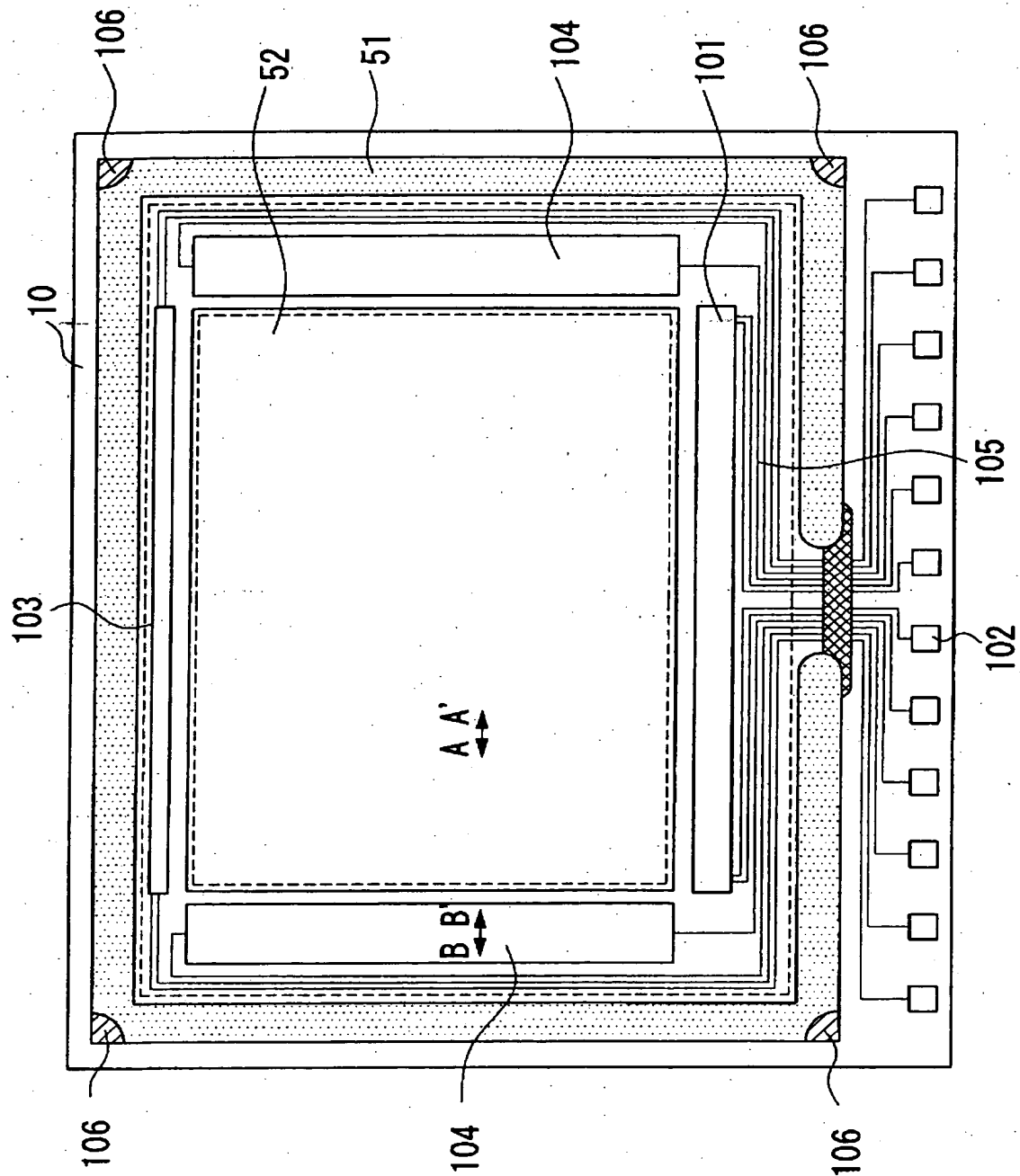


FIG. 2

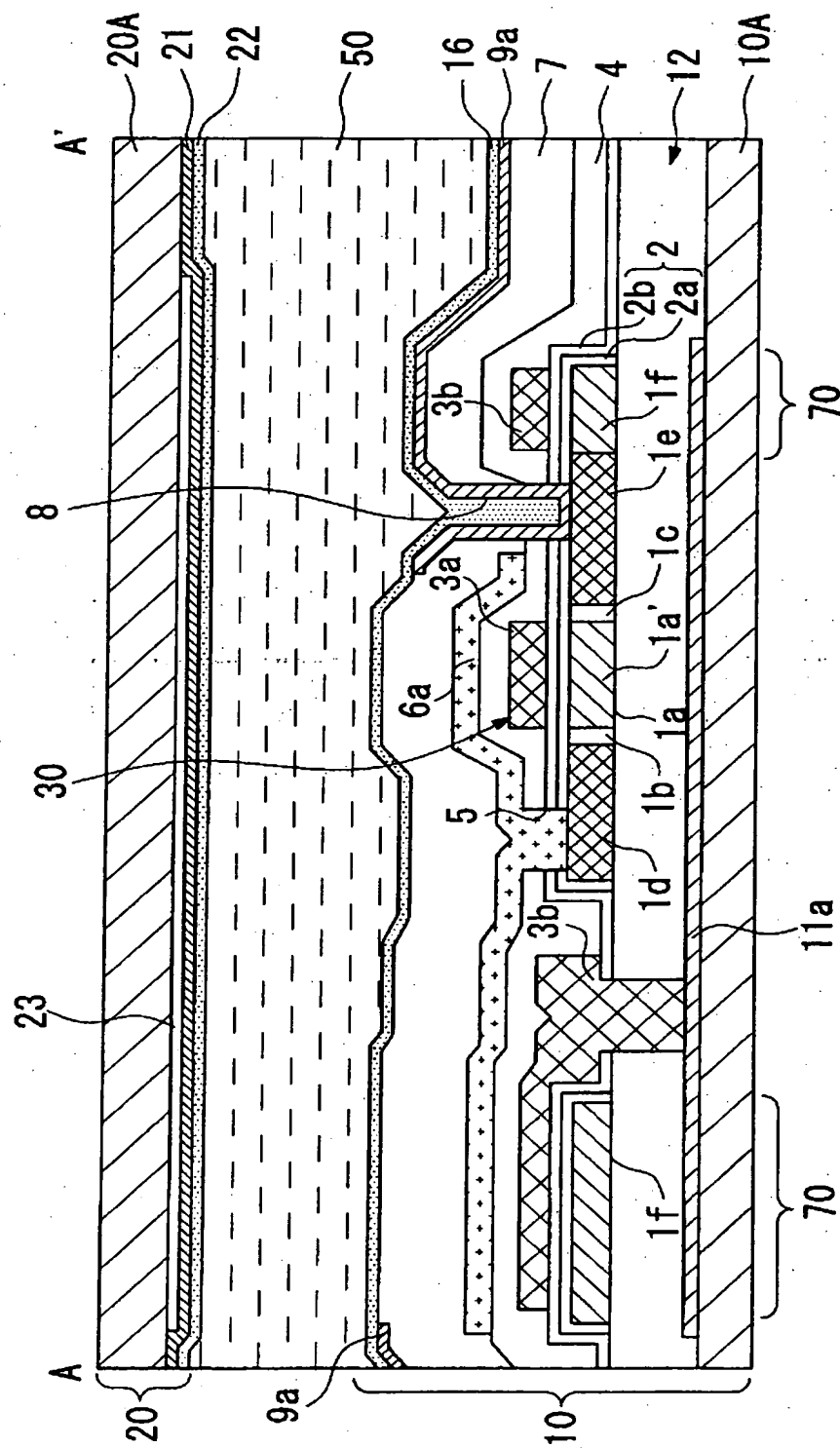


FIG. 3

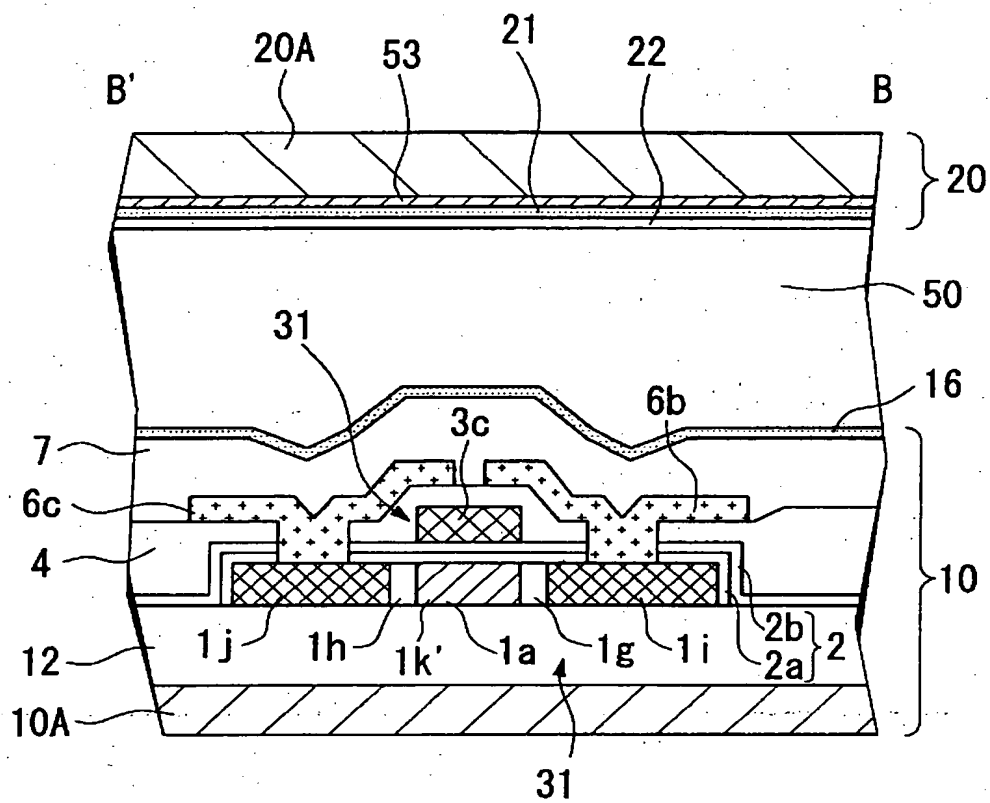


FIG. 4A

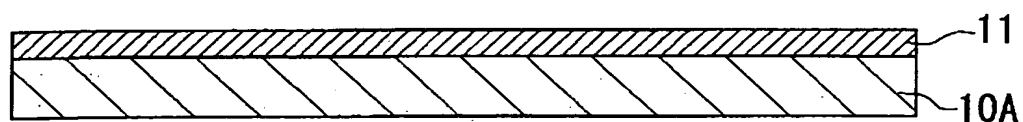


FIG. 4B

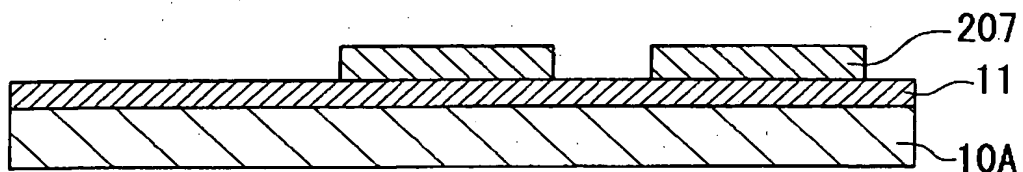


FIG. 4C

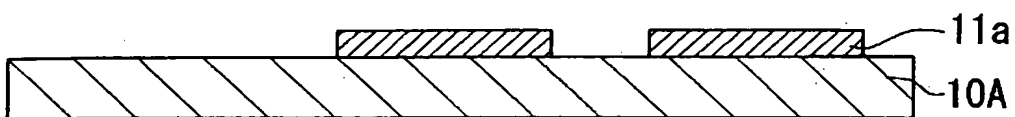


FIG. 5A

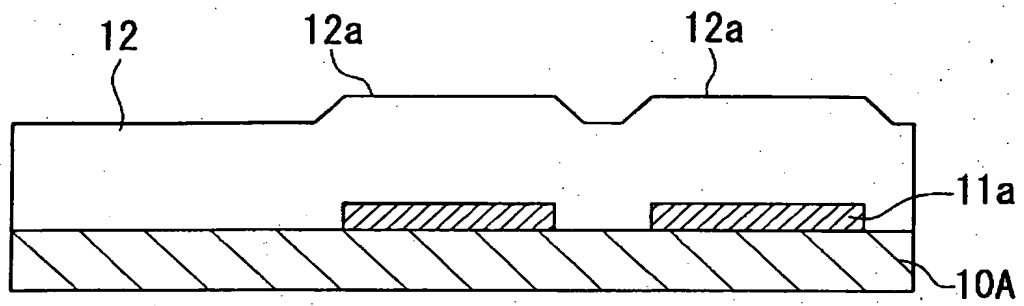
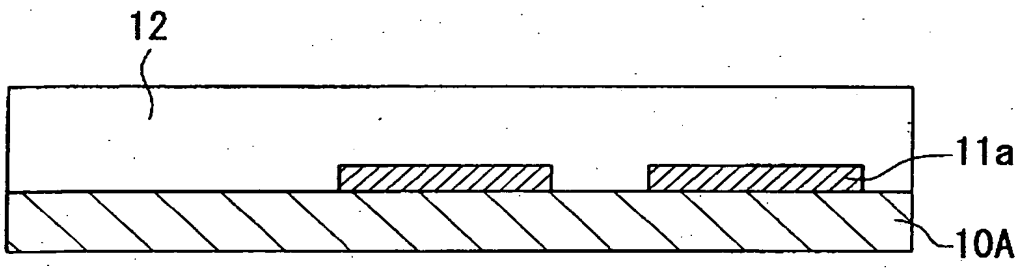


FIG. 5B



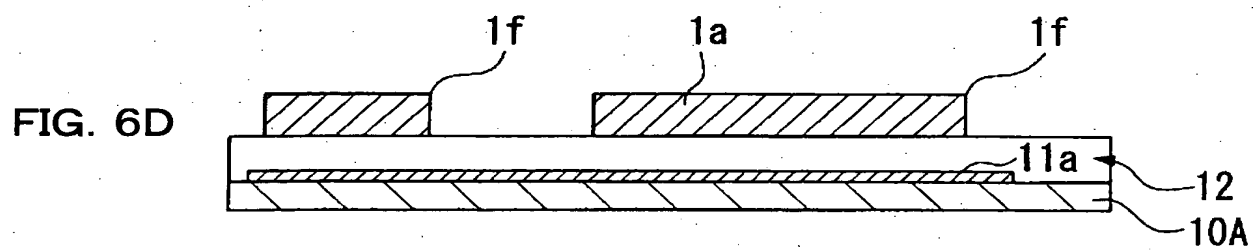
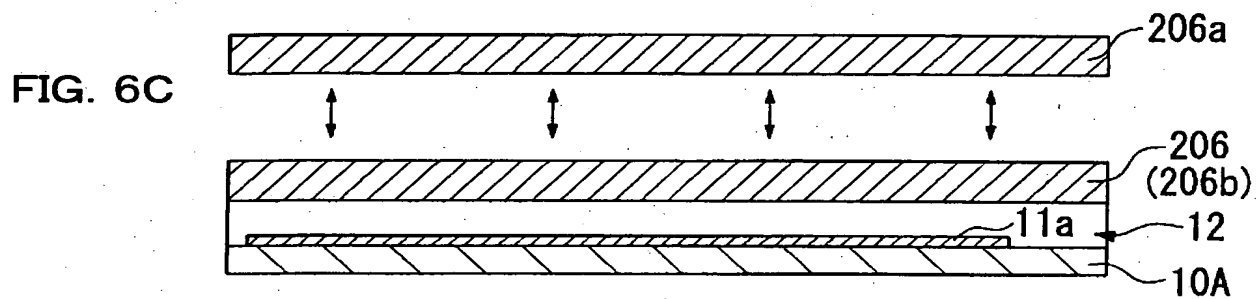
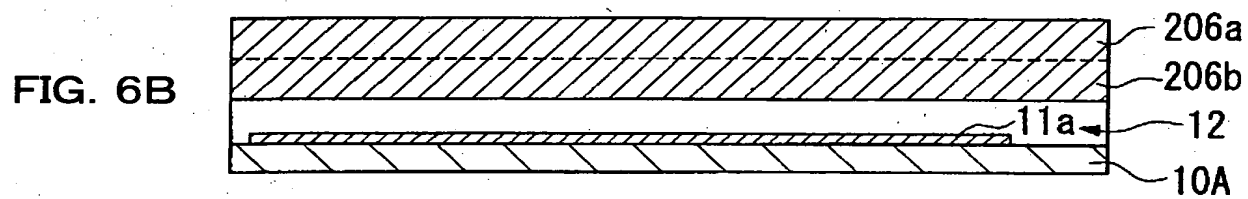
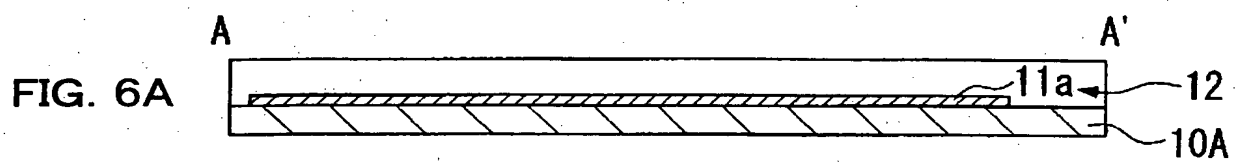


FIG. 7A

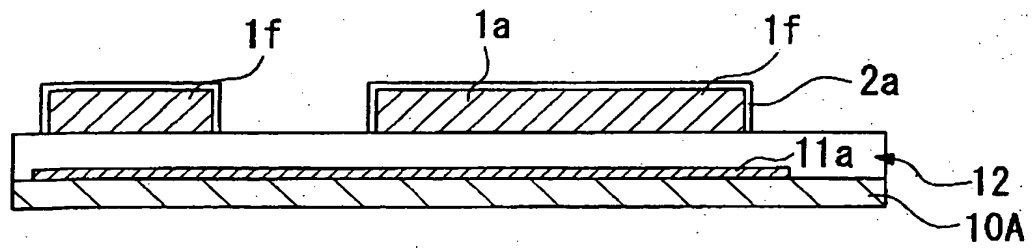


FIG. 7B

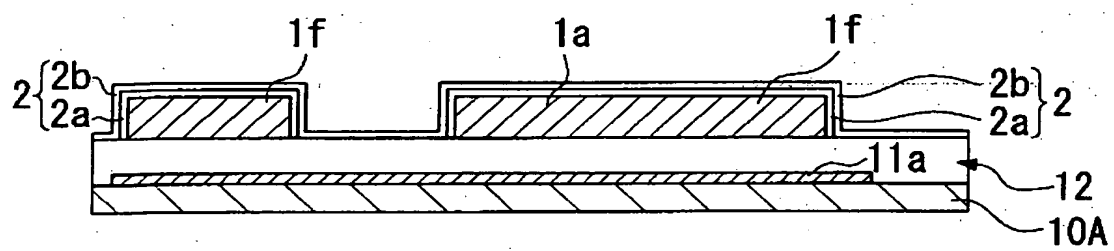


FIG. 8A

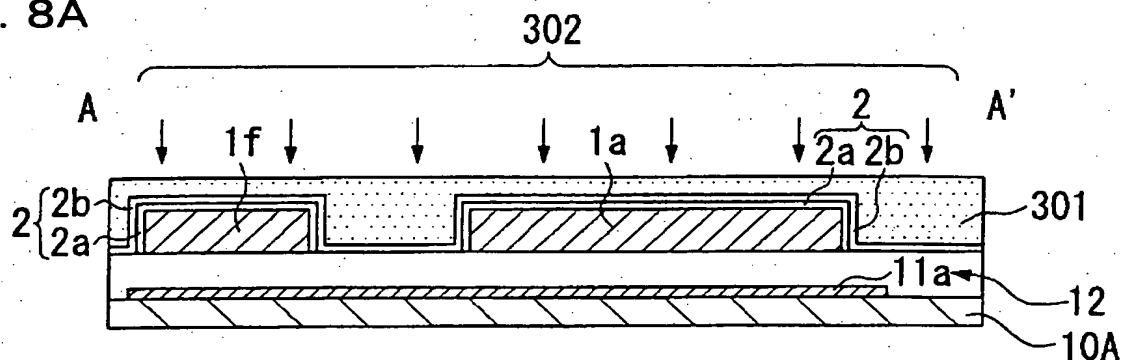


FIG. 8B

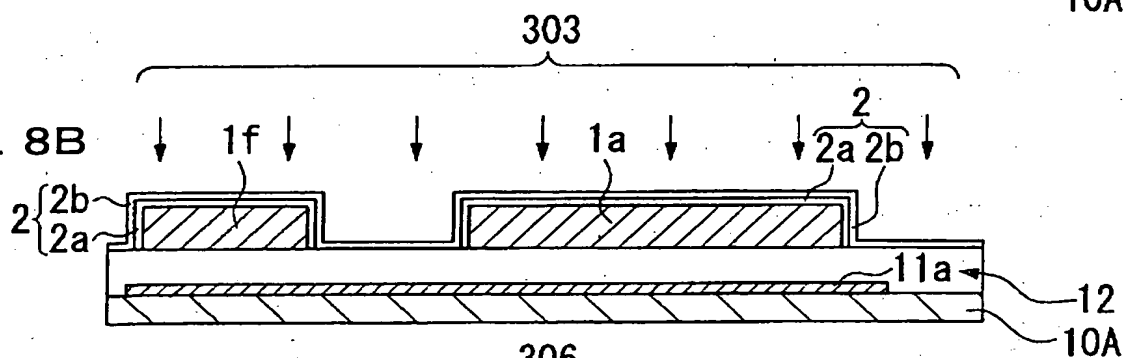


FIG. 8C

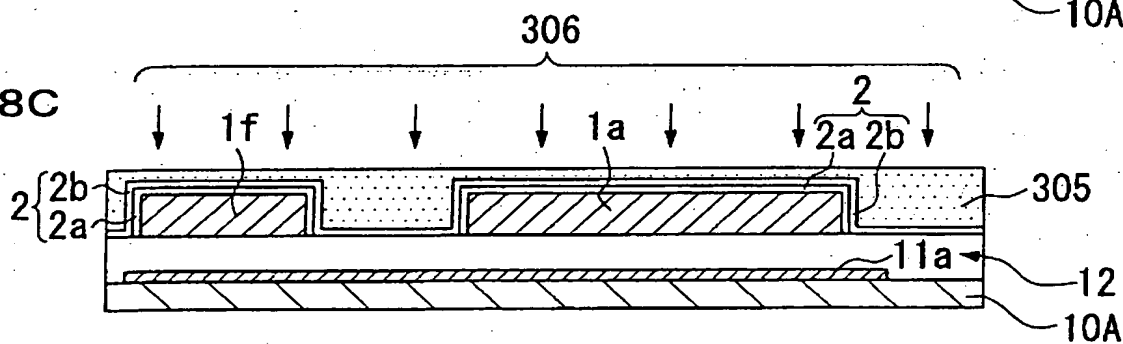
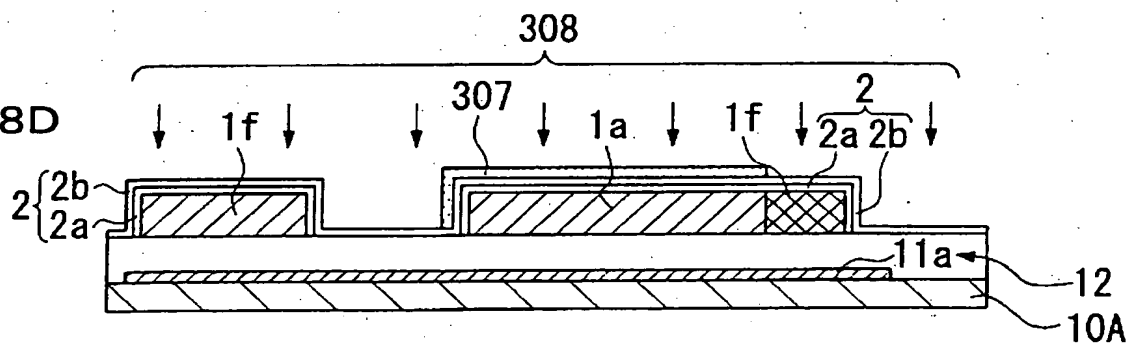
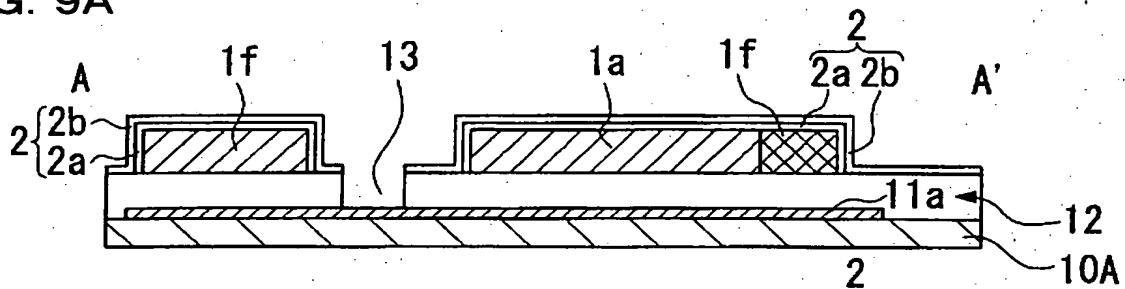


FIG. 8D



**FIG. 9A**



**FIG. 9B**

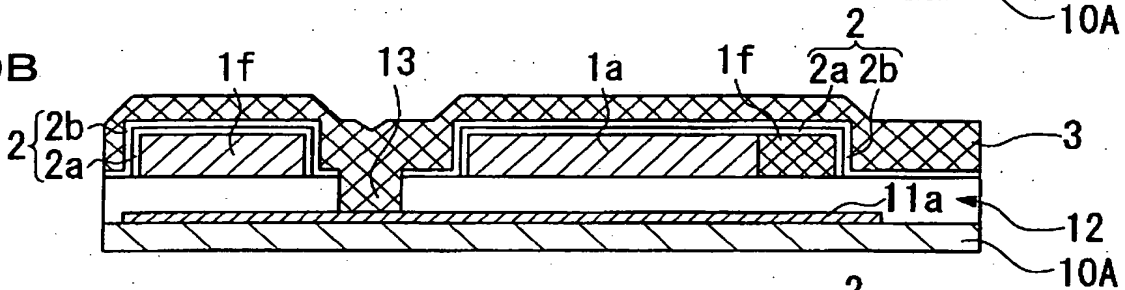


FIG. 9C

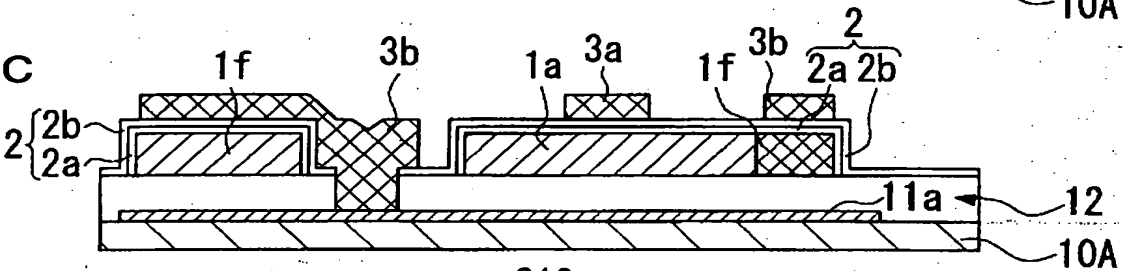
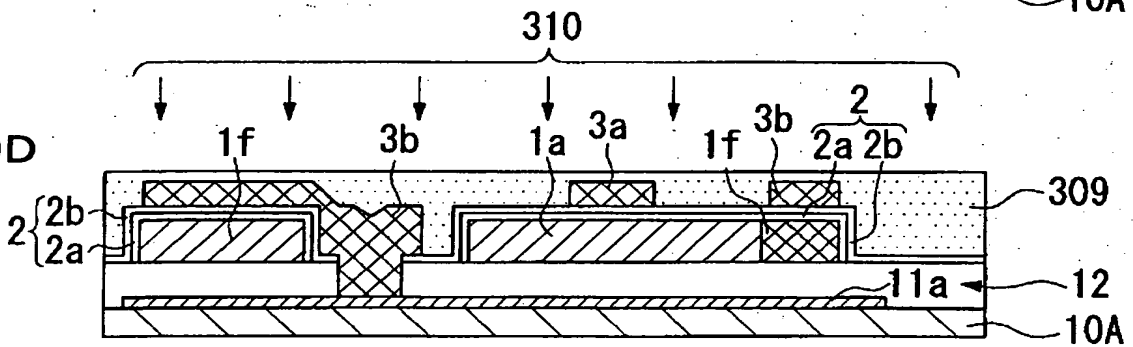


FIG. 9D



**FIG. 9E**

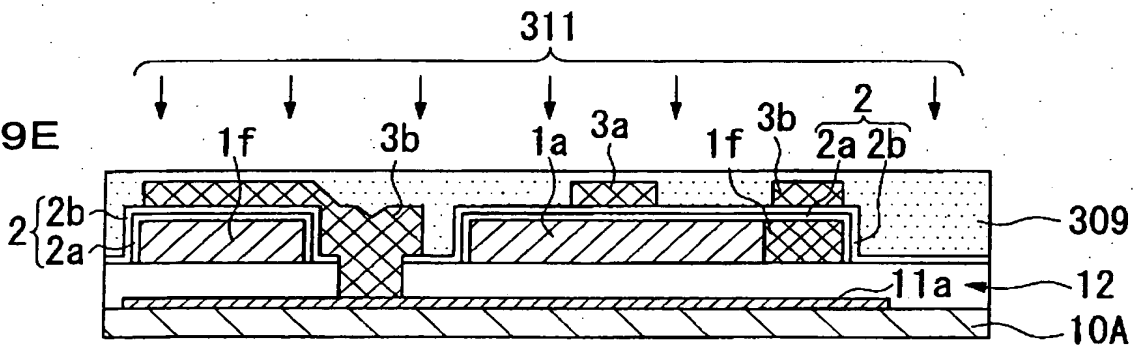




FIG. 10A

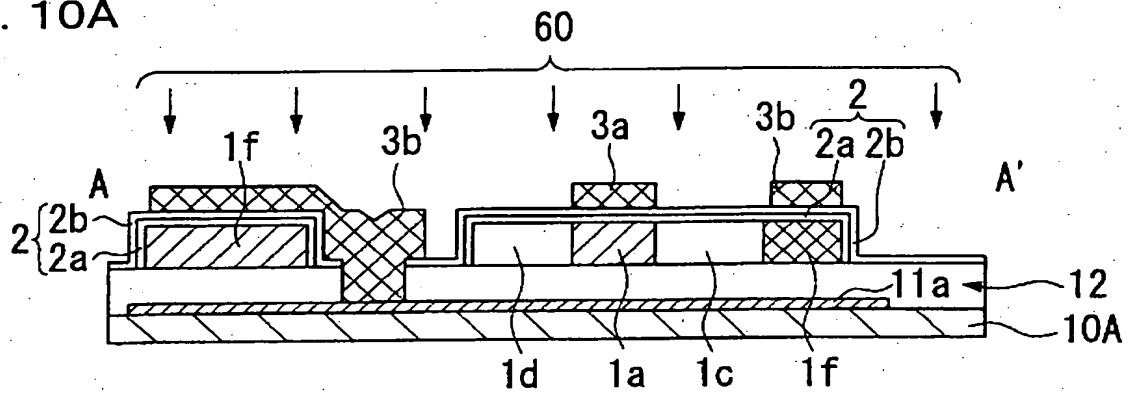


FIG. 10B

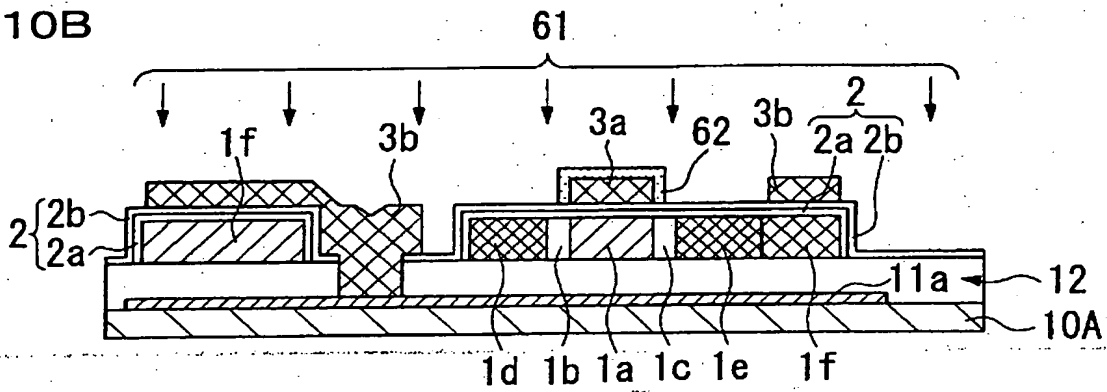


FIG. 10C

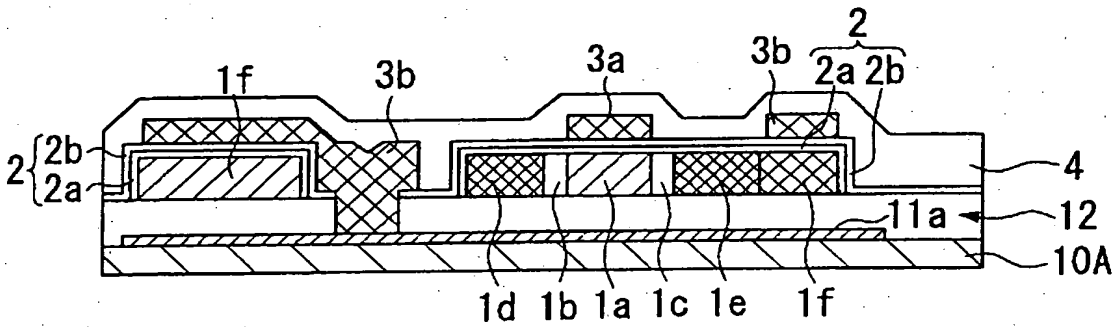


FIG. 10D

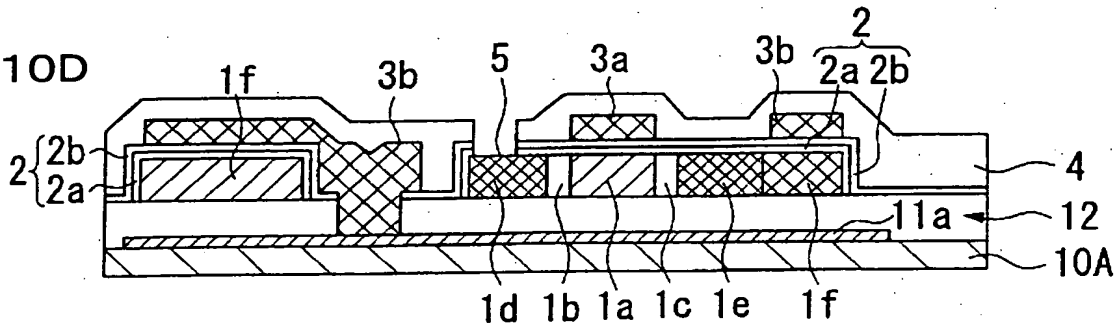


FIG. 11A

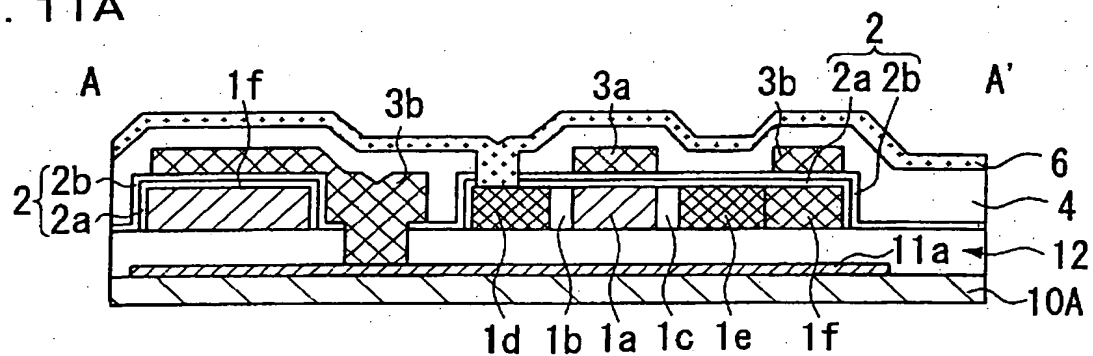


FIG. 11B

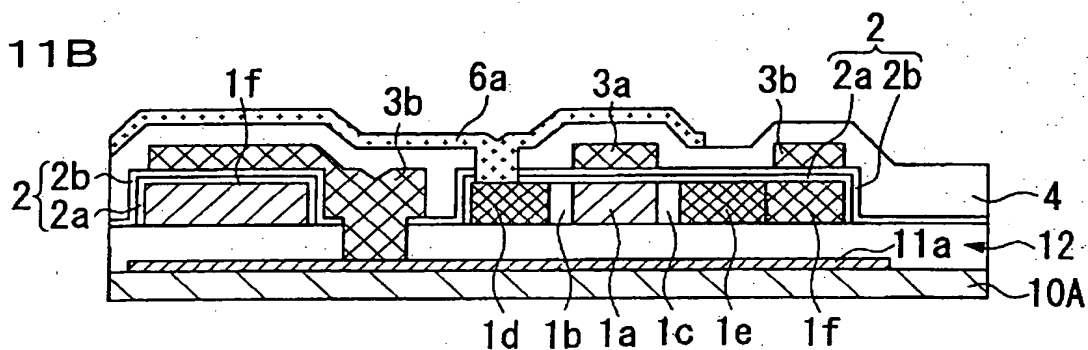
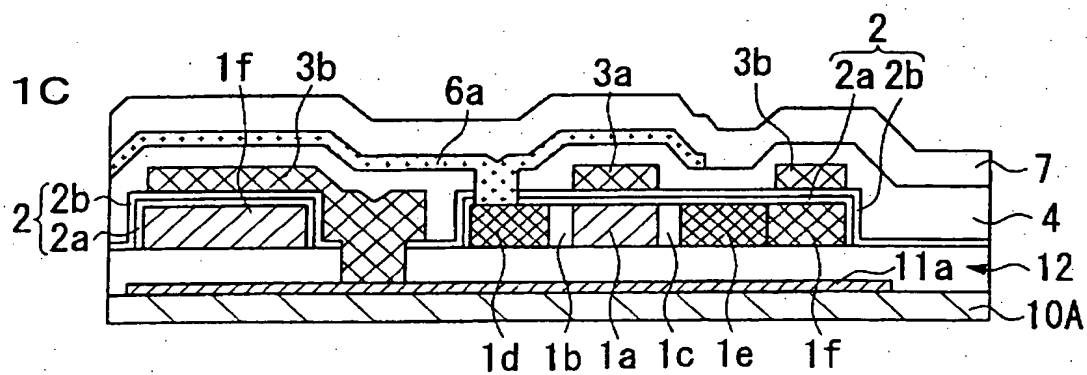


FIG. 11C



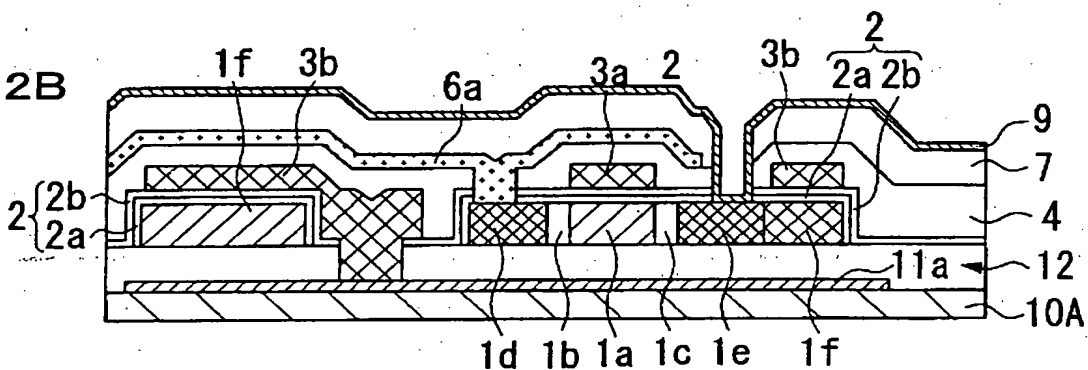


Fig. 2C is a cross-sectional view of the semiconductor device. It shows a substrate 10A with a base layer 12. A layer 4 is formed on the substrate, with a patterned layer 7 on top. A layer 9a is formed on the surface. A central region contains a stack of layers: 1f, 3b, 6a, 3a, 3b, and 2 (which is further divided into 2a and 2b). A layer 11a is located between the central stack and the substrate. The bottom of the device features a series of layers labeled 1d, 1b, 1a, 1c, 1e, and 1f. The entire structure is covered by a top layer 9a.

FIG. 13A

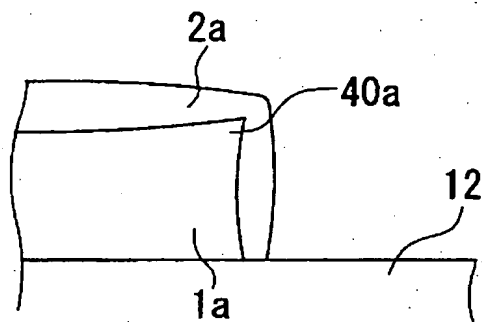


FIG. 13B

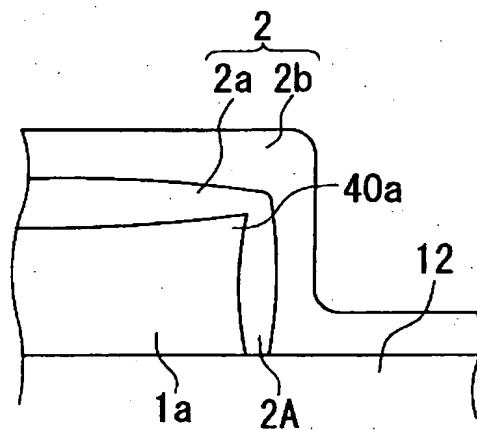


FIG. 14

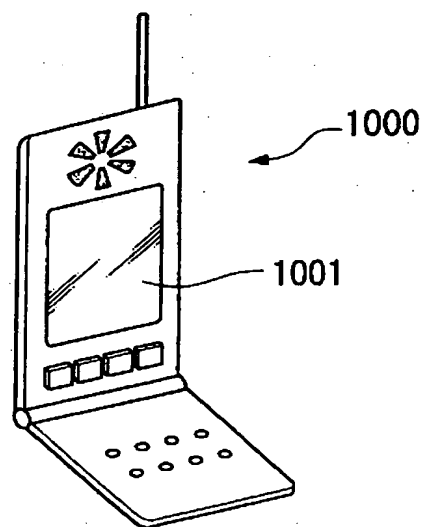


FIG. 15

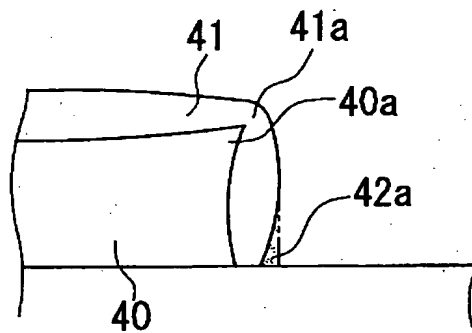


FIG. 16

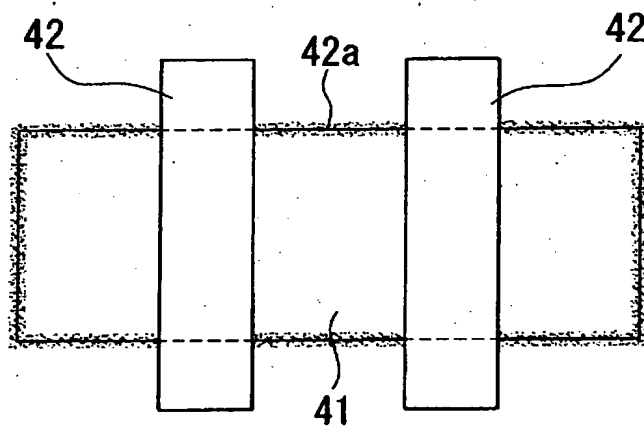


FIG. 17

